CLAIM AMENDMENTS

1. (previously presented) A method of converting a silicon on insulator (SOI) substrate into a strained SOI substrate, the method comprising the steps of:

providing an SOI substrate having a thin silicon layer and an insulator;

providing at least one first epitaxial relaxing layer on the SOI-substrate,

producing a defect region in a layer above the silicon layer of the SOI-substrate, and

relaxing the first layer by a thermal treatment in an inert atmosphere to simultaneously strain the silicon layer of the SOI-substrate via dislocation mediated strain transfer and to produce the strained silicon layer directly on the insulator.

2. (previously presented) The method according to claim 1, further comprising the step of

forming defects that give rise to relaxation of at least one neighboring layer of the layer which is to be strained.

3. (previously presented) The method according to claim 1, further comprising the step of

subjecting the layer structure for relaxation to a thermal treatment and/or oxidation.

4. (previously presented) The method according to claim 1, further comprising the step of

depositing the first layer upon the silicon layer to be strained.

5. (currently amended) The method according to claim 4 wherein the first layer has a different degree of ~~stress~~ strain than the silicon layer to be strained.

6. (previously presented) The method according to claim 4 wherein the defect region is produced in the first layer.

7 - 9. (canceled)

10. (currently amended) The method according to claim 1 wherein two neighboring layers of the layer to be strained have other degrees of ~~stress~~ strain than the layer to be strained.

11. (previously presented) The method according to claim 1 wherein a plurality of layers are relaxed.

12. (previously presented) The method according to claim 1 wherein a plurality of layers to be strained have strain transferred to them.

13. (previously presented) The method according to claim 1, further comprising the step of

depositing on the first layer epitaxially at least one second layer with a different lattice structure.

14. (previously presented) The method according to claim 13 wherein the defect region is produced in the second layer.

15. (previously presented) The method according to claim 1 wherein on the layer to which strain is to be transferred at least one graded layer is deposited as the first layer.

16. (previously presented) The method according to claim 15 wherein at the region of the layer to be strained, the graded layer has a degree of strain that is different from that of the layer to be strained.

17. (previously presented) The method according to claim 15, further comprising the step of

producing a defect region in the graded layer.

18. (previously presented) The method according to claim 1, further comprising the step of

depositing an epitaxial layer structure comprising a plurality of layers on the substrate.

19. (canceled)

20. (currently amended) The method according to claim 1 [[9]] wherein the thermal treatment is done at a temperature between 550 degrees and 1200 degrees C.

21. (currently amended) The method according to claim 1 [[9]] wherein the thermal treatment is done at a temperature between 700 degrees and 980 degrees C.

22 - 23. (canceled)

24. (previously presented) The method according to claim 1 wherein the relaxation is carried out over a limited region of a layer.

25. (previously presented) The method according to claim 1, further comprising the step of
applying a mask.

26 - 27. (canceled)

28. (previously presented) A method of converting a silicon on insulator (SOI) substrate into a strained SOI substrate, the method comprising the steps of:

providing an SOI substrate having a thin silicon layer and an insulator;

providing at least one first epitaxial relaxing layer on the SOI-substrate,

producing a defect region in a layer above the silicon layer of the SOI-substrate by ion implantation of hydrogen ions or helium ions with a dose of 3×10^{15} to 4×10^{16} cm^{-2}, and

relaxing the layer above the silicon layer by a thermal treatment to simultaneously strain the silicon layer of the SOI-substrate via dislocation mediated strain transfer and to produce the strained silicon layer directly on the insulator.

29 - 34. (canceled)

35. (previously presented) The method according to claim 13, further comprising out the step of

carrying out two implantations to produce two defect regions in the first layer and in the second layer.

36. (previously presented) The method according to claim 28, further comprising the step of

tilting the substrate during the ion implantation at an angle greater than 7°.

37. (canceled)

38. (previously presented) The method according to claim 1 wherein the defect region is produced by a change in the temperature during the formation of one of the layers.

39. (previously presented) The method according to claim 1 wherein the defects are produced in a Si-C layer by thermal treatment.

40 - 41. (canceled)

42. (previously presented) The method according to claim 1 wherein a silicon surface layer of the SOI substrate is the layer to be strained and the SiO_2 of the SOI substrate forms the insulator of the substrate.

43. (previously presented) The method according to claim 1 wherein an SIMOX or BESOI substrate is selected as a base structure for the substrate.

44. (previously presented) The method according to claim 1, further comprising the step of

selecting a silicon on sapphire as a base structure for the substrate.

45. (previously presented) The method according to claim 1 wherein the layer neighboring the silicon layer becomes viscous at a temperature required for the relaxation.

46 - 47. (canceled)

48. (previously presented) The method according to claim 1 Si-Ge or Si-Ge-C or Si-C as the material for the first layer which is deposited on the layer to be strained.

49. (canceled)

50. (previously presented) The method according to claim 13 wherein silicon as the material for the second layer which is deposited upon the first layer.

51. (previously presented) The method according to claim 15, further comprising the step of

selecting Si-Ge as the material for a graded layer.

52. (previously presented) The method according to claim 51 wherein the germanium concentration in the graded layer decreases from the interface with the layer to be strained to the surface of the graded layer.

53. (previously presented) The method according to claim 15 wherein the germanium concentration in a Si-Ge layer at the interface with the layer to be strained is 100 percent.

54. (canceled)

55. (previously presented) A method of converting a silicon on insulator (SOI) substrate into a strained SOI substrate, the method comprising the steps of:

providing an SOI substrate having a thin silicon layer and an insulator;

growing at least one first epitaxial relaxing layer on the SOI-substrate,

producing a defect region in a layer above the silicon layer of the SOI-substrate,

relaxing the layer above the silicon layer by a thermal treatment to simultaneously strain the silicon layer of the SOI-substrate via dislocation mediated strain transfer and to produce the strained silicon layer directly on the insulator, the

dislocation density after growth amounting to less than 10^5 cm^{-2}, and

selecting a total layer thickness of the layer structure that during growth of the epitaxial layer it does not substantially relax.

56. (previously presented) The method according to claim 1 wherein a layer to be strained has a thickness d_3 in the range of 1 to 50 nanometers.

57. (previously presented) The method according to claim 1 wherein the silicon layer to be strained has a thickness d_3 in the range of 5 to 30 nanometers.

58. (previously presented) The method according to claim 57 wherein the first layer has a thickness d_4 close to a critical layer thickness for pseudomorphic growth.

59. (previously presented) The method according to claim 58 wherein a layer thickness ratio d_4/d_3 is greater than about 10.

60. (previously presented) The method according to claim 13 wherein the second layer has a thickness d_5 = 50 nanometer to 1000 nanometer.

61. (previously presented) The method according to claim 13 wherein the second layer has a thickness d_5 = 300 nanometer to 500 nanometer.

62. (previously presented) The method according to claim 1 wherein the layer to be strained is locally strained.

63. (previously presented) The method according to claim 62 wherein the layer to be strained is locally strained in regions which are vertical in a plane with the defect region.

64. (previously presented) The method according to claim 13 wherein the defect region is produced at a spacing of 50 nanometers to 500 nanometers from the layer to be relaxed.

65. (previously presented) The method according to claim 1 wherein the defect region is at a spacing of 50 nanometers to 100 nanometers above the first layer on the layer to be strained.

66. (previously presented) The method according to claim 13, further comprising the step of

removing the first and second layers after producing the strained layer or after producing a strained region.

67. (previously presented) The method according to claim 1 wherein wet chemical material-selective etching is used.

68. (previously presented) The method according to claim 67, further comprising the step of
etching trenches in the depth of the silicon and epitaxial layers.

69. (previously presented) The method according to claim 68, further comprising the step, after producing the etched trenches, of
relaxing the first layer or a further layer by a thermal treatment.

70. (previously presented) The method according to claim 68, further comprising the step of
filling the trenches with insulating material to produce shallow trench insulation.

71. (previously presented) The method according to claim 1, further comprising the step of
carrying out at least one further thermal treatment for relaxation of at least one layer.

72. (previously presented) The method according to claim 1 wherein a strained layer or an unstrained layer are produced with a surface roughness of less than 1 nanometer.

73. (previously presented) The method according to claim 72 wherein a surface roughness of the layer is further reduced by the growth of a thermal oxide thereon.

74. (previously presented) The method according to claim 1, further comprising the step of

producing on a strained region of the layer an n- and/or p- MOSFET.

75. (previously presented) The method according to claim 1, further comprising the step of

depositing a further epitaxial layer comprising silicon or silicon/germanium or an Si-Ge-C layer or a germanium layer.

76. (previously presented) The method according to claim 1, further comprising the step of

producing on a strained silicon-germanium region p-MOSFETs as a further epitaxial layer or as a nonrelaxed layer structures.

77. (previously presented) The method according to claim 1, further comprising the step of

producing bipolar transistors on unstrained regions of the layer to be strained.

78. (previously presented) The method according to claim 77 wherein for producing a bipolar transistor, a silicon-germanium layer is applied.

79. (previously presented) The method according to claim 1, wherein the steps of claim 1 are carried out a plurality of times.

80 - 98. (canceled)

99. (new) The method according to claim 19 wherein the thermal treatment is carried out in nitrogen.

100. (new) The method according to claim 28 wherein at least two implantations are carried out.

101. (new) The method according to claim 100 wherein a hydrogen implantation is carried out in combination with a helium implantation.

102. (new) The method according to claim 32 wherein between two implantations a thermal treatment is carried out.

104. (new) The method according to claim 1 wherein the total layer thickness of the layer structure is so selected that during growth of the epitaxial layer it does not produce any noticeable relaxation.